REMARKS

Claims 1-21 and 23-33 are pending in the present application. Claim 22 is cancelled herein. Claims 32 and 33 have been added, and claims 1-21 and 23-31 have been amended. No new matter has been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

The Examiner has objected to the Information Disclosure Statement (IDS) filed March 30, 2004 as failing to comply with 37 C.F.R. § 1.98(a)(3). In particular, the Examiner objected to the two German patents listed in the IDS. Applicant has filed a revised IDS herewith that includes translations of the abstract portions of two German patents. The German patents were cited in the corresponding German application. Applicant does not have a full translation of the cited German patents.

The Examiner has objected to the Specification under 37 C.F.R. § 1.77(b) because the disclosure includes only one heading. Applicant has submitted herewith clean and marked-up versions of an Amended Specification, which adds headings and an Abstract to the specification as filed. The claims in the Amended Specification reflect the claim amendments included in the present Amendment. No new matter has been added by the amendments to the specification or claims.

The Examiner has objected to claim 17 because the acronyms "PLD" and "PLA" are not defined in the claim. Applicant has amended claim 17 and the Amended Specification to clarify that "PLDs" refer to programmable logic devices and "PLAs" refer to programmable logic arrays as noted by the Examiner in the Office Action.

The Examiner has rejected claim 17 under 35 U.S.C. § 112, second paragraph, as combining a broad limitation together with a narrow limitation that falls within the broad

limitation. Applicant has amended claim 17 to include the limitations PLA and PLD, and added new claims 32 and 33 to include the limitations functional memory devices and fundamental memory devices, respectively. No new matter has been added by these amendments.

Claims 1, 8, 10-12, 18-21 and 27-29 have been rejected under 35 U.S.C. § 102(b) as assertedly being anticipated by U.S. Patent No. 5,508,653 to Chu *et al.* (hereinafter "Chu"). Claims 22-26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chu in view of U.S. Patent No. 6,600,220 to Barber *et al.* (hereinafter "Barber"). Claims 1 and 8 have been alternately rejected under 35 U.S.C. § 102(a) as assertedly being anticipated by Nishikawa *et al.* (JP 2002-333687) using U.S. Publication No. 2004/0094820 as a translation (hereinafter "Nishikawa"). Claims 2-7, 9-11, 18, 19, 22-25 and 27-31 have been alternately rejected under 35 U.S.C. § 103(a). Applicant respectfully traverses these rejections.

Claim 1 has been amended to incorporate elements of claim 22, which is now canceled. Claim 1, as amended, requires that:

> the system is adapted such that, in a first operating mode of the second semiconductor device, the voltage supply device of said second semiconductor device provides the supply voltage for the second semiconductor device, and, in a second operating mode of the second semiconductor device, the voltage supply device of said first semiconductor device provides the supply voltage for the second semiconductor device.

The Examiner points to features of Barber and Nishikawa as teaching or suggesting these features.

Barber does not teach or suggest the required elements of claim 1. Barber teaches that two integrated circuit chips (38) share signal terminals (62). The Examiner mistakenly identifies signal terminals (62) as semiconductors. Office Action at 11. The Examiner further suggests that the semiconductors "communicate power signals between each other in one operation." *Id.*

The cited section of Barber at column 8 does not support the Examiner's rejection. Barber teaches that each integrated circuit chip (38) has its own voltage converter (42) that it receives power signals from via power terminals (64). As illustrated in Figure 5, and discussed in column 8, Barber does not teach that one integrated circuit chip (38) is capable of receiving power from more than one power supply (42). Moreover, there is no suggestion that such a feature is necessary or possible in Barber, nor is there any suggestion as to how such a power-sharing arrangement would be accomplished in the circuit of Figure 5.

Nishikawa also fails to teach or suggest the required elements of claim 1. Nishikawa teaches that one plurality of components 201e-206e belong to one path 20p; and that a second plurality of components 207e-209e belong to another path 21p. Nishikawa at [0093]-[0097] and Figure 2A. Paths 20p and 21p have different signal delay values. *Id.* Power supply 11 provides voltage VDD1 to components 201e-206e; and power supply 12 provides voltage VDD2 to components 207e and 208e. *Id.* Power supply 11 also provides voltage VDD1 to component 209e, which continues to operate on path 21p without a deterioration of performance. *Id.* Nishikawa fails to teach or suggest that a second semiconductor device, such as 209e, has two operating modes. Instead, in Nishikawa, all of the components of Figure 2A have one operating mode defined by either path 20p or 21p. There is no teaching or suggestion in Nishikawa that a second operating mode is possible, nor is there any teaching or suggestion as to how the components would be connected to a different path (20p, 21p) than the assigned path. Furthermore, as shown in Figure 2A of Nishikawa, component 209e is hardwired (solid black line) to power supply 11 and there is no teaching or suggestion as to how component 209e can be connected to power supply 11. Moreover, there is no teaching or suggestion that such as change between power supplies (11, 12) would take place based upon a change in operating modes.

Accordingly, Applicant respectfully submits that claim 1 is allowable over the cited references and requests that the claims be passed to issue.

Claims 2-21 and 23-33 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner please contact Applicant's attorney at the address below. In the event that the enclosed fees are insufficient, please charge any additional fees required to keep this application pending, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

5/14/07
Date

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~~DESCRIPTION~~

TITLE

Semiconductor Device Voltage Supply for a System With at Least Two, Especially Stacked, Semiconductor Devices

[0001] This application claims priority to German Patent Application DE 10315303.9, which was filed April 2, 2003.

TECHNICAL FIELD

[0002] ~~In accordance with the preamble of claim 1, the~~ The invention relates to a system with two - especially stacked - semiconductor devices and a semiconductor device voltage supply for such a system, respectively.

[0010] A reference voltage - which is subject to relatively minor fluctuations only - is applied to the positive input of the differential amplifier. The voltage output at the drain of the field effect transistor may be fed back to the negative input of the differential amplifier directly, or e.g. by the interposition of a voltage divider.

[0011] The differential amplifier regulates the voltage available at the gate connection of the field effect transistor such that the (fed back) drain voltage - and thus the voltage output by the voltage regulator - is constant and as high as the reference voltage, or e.g. by a certain factor higher.

[0012] Semiconductor devices are usually incorporated in appropriate housings, e.g. appropriate surface mountable housings (SMD housings) or plug mountable housings (e.g. corresponding Dual-In-Line (DIL) housings, Pin-Grid-Array (PGA) housings, etc.).

[0013] In one single housing, there may also be arranged two or more semiconductor devices instead of only one single semiconductor device.

[0014] In the case of memory devices, in particular DRAMs for increasing the storage density, several semiconductor devices may, for instance, be mounted in a stacked manner in one single housing.

[0015] For instance, two 256 Mbit memory devices may be provided in one single housing, this effecting a 512 Mbit chip.

[0016] The semiconductor devices, in particular memory devices, provided in one single housing comprise voltage supply means that are independent of one another.

[0017] When a memory device is accessed (i.e. when corresponding external data are stored on the memory device, or when data that are stored on the memory device are read

out), there will flow, in general, relatively high currents that are generated by the corresponding voltage supply means.

[0018] Contrary to this, only relatively low currents will flow in standby or refresh operation (e.g. for supplying leakage currents or operating currents).

[0019] The standby or refresh currents each may, for instance, be in the range of approx. 50 μA - i.e. amount to a total of 100 μA in the case of e.g. two stacked memory devices (with the operating currents of the respective voltage supply means constituting the major part of these currents).

BRIEF SUMMARY OF THE INVENTION

[0020] It is an object of the invention to provide a novel system with two - especially stacked - semiconductor devices, and - in particular - a semiconductor device voltage supply for such a system, respectively.

[0021] The invention achieves this and further objects by the subject matter of claim 1.

[0022] Advantageous further developments of the invention are indicated in the subclaims.

[0023] In accordance with a basic idea of the invention, a system, in particular a semiconductor device system, is provided, comprising

[0024] - a first semiconductor device, and

[0025] - a second semiconductor device,

[0026] wherein the first semiconductor device comprises a voltage supply means, and wherein the voltage supply means of the first semiconductor device is connected to the second semiconductor device, so that the voltage supply means of the first semiconductor device can provide a supply voltage for the second semiconductor device.

[0027] It is of particular advantage when the second semiconductor device additionally also comprises a voltage supply means.

[0028] Preferably, in a first operating mode of the second semiconductor device, the voltage supply means of the second semiconductor device provides the voltage supply for the second semiconductor device, and in a second operating mode of the second

semiconductor device - in particular in a standby or refresh mode -, this is effected by the voltage supply means of the first semiconductor device.

[0029] The voltage supply means of the second semiconductor device may then be deactivated, so that the operating current thereof may be saved (and thus, altogether, the currents required for operating the semiconductor devices).

[0030] In an advantageous development of the invention, the first semiconductor device and the second semiconductor device are arranged in one and the same housing.

[0031] Preferably, the first and second semiconductor devices are arranged in the housing in a stacked manner.

[0032] Advantageously, the housing may be a plug mountable semiconductor device housing, or e.g. a surface mountable semiconductor device housing.

[0033] It is particularly preferred when the first and/or the second semiconductor devices are corresponding memory devices, in particular corresponding DRAM memory devices.

[0034] In an advantageous development of the invention, the voltage supply means of the first semiconductor device is connected to a corresponding pad of the first semiconductor device.

[0035] Preferably, the pad of the first semiconductor device is connected to a corresponding pad of the second semiconductor device, which the voltage supply means of the second semiconductor device can be connected to.

[0036] The pad of the first semiconductor device may, for instance, be connected directly to the corresponding pad of the second semiconductor device, in particular by means of an appropriate bonding wire.

[0037] Alternatively, the pad of the first semiconductor device may, for instance, also be connected to the corresponding pad of the second semiconductor device indirectly, e.g. via an interposer.

BACKGROUND

[0003] Semiconductor devices, in particular memory devices such as DRAMS (DRAM = Dynamic Random Access Memory or dynamic read-write-memory, respectively) in general comprise one or several voltage supply means.

[0004] A voltage supply means serves to generate, from an - externally provided - voltage, a voltage used internally in the semiconductor device.

[0005] The voltage level of the internal voltage generated by the semiconductor device voltage supply means may differ from the level of the external voltage.

[0006] In particular, the internally used voltage level may be lower than the externally used voltage level.

[0007] An internal voltage level that is reduced vis-à-vis the externally used voltage level has, for instance, the advantage that the power loss in the semiconductor device can be reduced.

[0008] Furthermore, the external voltage may be subject to relatively strong fluctuations. Therefore, a so-called voltage regulator is frequently used as voltage supply means, which - in order that the device may be operated without fault - converts the external voltage into an internal voltage that is subject to relatively minor fluctuations only and is regulated at a particular, constant (possibly reduced) value.

[0009] Conventional voltage regulators may, for instance, comprise a differential amplifier and a field effect transistor. The gate of the field effect transistor may be connected to an output of the differential amplifier, and the source of the field effect transistor may e.g. be connected to the external voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] In the following, the invention will be explained in detail by means of several embodiments and the enclosed drawing. The drawing shows:

[0039] Figure 1a is a schematic representation of a system with two stacked semiconductor devices with a semiconductor device voltage supply in accordance with a first embodiment of the present invention; and

[0040] Figure 1b is a schematic representation of a system with two stacked semiconductor devices with a semiconductor device voltage supply in accordance with a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0041] List of Reference Signs

[0042] 1 semiconductor device system

[0043] 2a semiconductor device

[0044] 2b semiconductor device

[0045] 3a voltage supply means

[0046] 3b voltage supply means

[0047] 4 semiconductor device housing

[0048] 5a semiconductor device pad

[0049] 5b semiconductor device pad

[0050] 5c semiconductor device pad

[0051] 5d semiconductor device pad

[0052] 6 bonding wire

[0053] 6a bonding wire

[0054] 6b bonding wire

[0055] 7a line

[0056] 7b line

[0057] 7c line

[0058] 7d line

[0059] 8 activating/deactivating control means

[0060] 9 interposer

[0061] 10 connection

[0062] Figure 1a is a schematic representation of a system 1 with two stacked semiconductor devices 2a, 2b in accordance with a first embodiment of the present invention.

[0063] The two semiconductor devices 2a, 2b are - apart, in particular, from the components serving for voltage supply of the semiconductor devices 2a, 2b or controlling the voltage supply, respectively, which will be explained in more detail in the following - substantially of identical structure.

[0064] The semiconductor devices 2a, 2b may, on principle, be any type of logic and/or memory devices, e.g. functional memory devices, in particular programmable logic devices (PLDs) or programmable logic arrays (PLAs), or e.g. table memory devices, in particular ROM or RAM table memory devices, etc.

[0065] For instance, appropriate DRAM table memory devices, e.g. a 256 Mbit, a 512 Mbit, or a 1 Gbit DRAM table memory device 2a, 2b, for instance appropriate DDR-DRAMs (Double Data Rate DRAMs), may be used as semiconductor devices 2a, 2b.

[0066] As is illustrated schematically in Figure 1a, the semiconductor devices 2a, 2b are arranged in the same semiconductor device housing 4.

[0067] The housing 4 may, for instance, be an appropriate plug mountable semiconductor device housing, e.g. a Dual-In-Line (DIL) housing, a Pin-Grid-Array (PGA) housing, etc., or a surface mountable semiconductor device housing (SMD housing), etc.

[0068] As results further from Figure 1a, the semiconductor devices 2a, 2b are mounted in the housing 4 such that they are substantially stacked.

[0069] By the stacking of the semiconductor devices 2a, 2b in the same housing 4, the system 1 can - e.g. when two 256 Mbit memory devices 2a, 2b are used as semiconductor devices 2a, 2b - altogether be used as a 512 Mbit memory device (or e.g. when two 512 Mbit memory devices are used, as a 1 Gbit memory device, etc.).

[0070] As is further illustrated in Figure 1a, each semiconductor device 2a, 2b comprises a voltage supply means 3a, 3b having a structure similar to that of conventional voltage supply means (or – alternatively - a plurality of, e.g. two, three, four, five, six, or seven, voltage supply means having a structure corresponding to that of the voltage supply means 3a, 3b).

[0071] The voltage supply means 3a, 3b serve to generate, from an external voltage - provided by a voltage source (not illustrated) arranged externally of the semiconductor devices 2a, 2b and of the housing, respectively - a corresponding internal voltage - used, for instance, internally in the respective semiconductor device 2a, 2b (cf. explanations below).

[0072] The external voltage provided by the external voltage source may, for instance, be supplied to the voltage supply means 3a, 3b via one or a plurality of supply pins (not illustrated) of the semiconductor device housing 4, and via semiconductor device pads connected therewith (e.g. the pads 5c, 5d illustrated in Figure 1a), as well as via corresponding lines 7a, 7b connected to the pads 5c, 5d or extending in the semiconductor devices 2a, 2b, respectively.

[0073] As voltage supply means 3a, 3b, e.g. appropriate charge pumps may be used that have a structure similar to that of conventional charge pumps, or e.g. - as in the embodiment illustrated here - voltage regulating means 3a, 3b that have a structure similar to that of conventional voltage regulating means.

[0074] These means serve to convert the external voltage - which may be subject to relatively strong fluctuations--into the above-mentioned internal voltage - which is subject to relatively minor fluctuations only and is regulated at a particular, constant value.

[0075] The internal voltage may, for instance, have substantially the same, or alternatively e.g. a lower, voltage level as/than the external voltage. The external voltage may, for instance, lie in the range of between 1.5 V and 2.5 V, e.g. at 1.8 V, and the internal voltage e.g. in the range of between 1.3 V and 2.0 V, e.g. at 1.5 V.

[0076] The voltage supply means 3a, 3b or voltage regulating means 3a, 3b, respectively, each may, for instance, comprise a differential amplifier and a field effect transistor. The gate of the field effect transistor may be connected to an output of the differential amplifier, and the source of the field effect transistor may be connected e.g. to the above-mentioned external voltage.

[0077] A reference voltage that is subject to relatively minor fluctuations only is applied to the positive input of the differential amplifier. The voltage output at the drain of the field effect transistor may be fed back to the negative input of the differential amplifier directly, or e.g. by the interposition of a voltage divider.

[0078] The differential amplifier regulates the voltage available at the gate connection of the field effect transistor such that the (fed back) drain voltage - and thus the voltage output by the corresponding voltage supply means 3a, 3b or voltage regulating means 3a, 3b, respectively, e.g. at corresponding lines 7c, 7d or connections, respectively (i.e. the above-mentioned voltage used internally on the semiconductor devices 2a, 2b (internal voltage)) - is constant and as high as the reference voltage, or e.g. by a certain factor higher.

[0079] The first and the second semiconductor devices 2a, 2b are operated in several, different modes.

[0080] In a first mode (working mode), an external access to the first or second semiconductor device 2a, 2b may, for instance, be effected (similar as with conventional memory devices). In so doing, corresponding – external - data may, for instance, be stored on the first or second semiconductor device 2a, 2b (with the data being input e.g. at corresponding pins of the semiconductor device housing 4), or data stored on the first or second semiconductor device 2a, 2b may be read out externally (with the data being output at corresponding pins of the semiconductor device housing 4).

[0081] A second operating mode may, for instance, be a standby mode (similar as with conventional memory devices), or, e.g. a refresh mode (also similar as with conventional memory devices).

[0082] During a refresh mode (or more exactly: during a refresh operation), the capacitors of the memory cells on which the data stored on the semiconductor devices 2a, 2b are stored, are correspondingly refreshed.

[0083] A refresh cycle may be performed at regular time intervals, e.g. every 1 to 10 ms or every 10 to 1000 ms, etc.

[0084] As will be explained in more detail in the following, in the semiconductor device system 1 illustrated in Figure 1a, the voltage supply means 3b of the second semiconductor device 2b is activated in the above-mentioned first operating mode (and possibly in one or several further operating mode(s)) - e.g. during the above-mentioned working mode -, and in the above-mentioned second operating mode (and possibly in one or several further operating mode(s)) - e.g. during the standby mode and/or during the refresh mode - the voltage supply means 3b of the second semiconductor device 2b is deactivated.

[0085] This happens e.g. by corresponding activating/deactivating signals being fed to the voltage supply means 3b of the second semiconductor device 2b by an activating/deactivating control means 8.

[0086] In the activated state, the voltage supply means 3b of the second semiconductor device 2b is switched on (is, in particular, connected to the supply or external voltage, so that corresponding operating currents - e.g. of between 20 μA and 80 μA, e.g. 50 μA - are flowing), and in the deactivated state it is switched off (is, in particular, separated from the supply or external voltage, so that corresponding operating currents are prevented from flowing).

[0087] As is further illustrated in Figure 1a, the voltage supply means 3a of the first semiconductor device 2a is connected - here: via the line 7c - to a corresponding semiconductor device pad 5a of the first semiconductor device 2a.

[0088] The pad 5a is connected to a corresponding semiconductor device pad 5b of the second semiconductor device 2b by means of a bonding wire 6.

[0089] The pad 5b of the second semiconductor device 2b is connected - here: via the line 7d - to the voltage supply means 3b of the second semiconductor device 2b (or to a line or a connection, respectively, at which - in the activated state of the voltage supply means 3b of the second semiconductor device 2b - the internal voltage then generated thereby is output).

[0090] By the above-described connection of the voltage supply means 3a of the first semiconductor device 2a to the second semiconductor device 2b it is achieved that, in the above-mentioned second operating mode of the second semiconductor device 2b (and possibly in one or several further operating mode(s)) - e.g. during the standby mode and/or during the refresh mode -, the voltage supply means 3a of the first semiconductor device 2a can, in addition to the – internal - supply voltage (internal voltage) for the first semiconductor device 2a, provide the – internal - supply voltage (internal voltage) for the second semiconductor device 2b.

[0091] In other words, in the above-mentioned second operating mode the voltage supply means 3a of the first semiconductor device 2a generates the respectively required (internal) voltages for both semiconductor devices 2a, 2b - the voltage supply means 3b of the second semiconductor device 2b is deactivated, so that the operating current thereof may be saved (this, altogether, reducing the currents required for operating the semiconductor devices 2a, 2b).

[0092] Contrary to this--as has already been explained above - in the above-mentioned first operating mode of the second semiconductor device 2b (and possibly in

one or several further operating mode(s)) - e.g. during the working mode - the voltage supply means 3b of the second semiconductor device 2b is put to an active state (and the voltage supply means 3a of the first semiconductor device 2a is possibly additionally separated from the voltage supply means 3b of the second semiconductor device 2b, or the above-mentioned line or the connection, respectively, at which the voltage supply means 3b of the second semiconductor device 2b outputs the internal voltage generated thereby (e.g. by controlling the activating/deactivating control means 8, or alternatively e.g. a corresponding control means provided on the first semiconductor device 2a)).

[0093] By this it is achieved that, in the above-mentioned first operating mode of the second semiconductor device 2b (and possibly in one or several further operating mode(s))--e.g. during the first working mode - the voltage supply means 3b of the second semiconductor device 2b provides the - internal - supply voltage (internal voltage) for the second semiconductor device 2b (and the voltage supply means 3a of the first semiconductor device 2a the – internal - supply voltage (internal voltage) for the first semiconductor device 2a).

[0094] Advantageously, the first and the second semiconductor devices 2a, 2b are - in particular until passing through the device function adjusting step which will be explained in more detail in the following - (at first) of substantially identical structure.

[0095] By means of the device function adjusting step it is determined during the manufacturing of the semiconductor devices whether a corresponding semiconductor device is to fulfill a function that corresponds to the function of the above-mentioned first semiconductor device 2a, i.e. the function of a "master" which, in the above-mentioned second operating mode (and possibly in one or several further operating mode(s)), is to

provide - in addition to its own voltage supply - the respectively required (internal) voltage also for one or several further semiconductor device(s), or a function corresponding to the function of the above-mentioned second semiconductor device 2b, i.e. the function of a "slave" which is to obtain, in the above-mentioned second operating mode (and possibly in one or several further operating mode(s)) the respectively required (internal) voltage from another semiconductor device ("master").

[0096] For determining the function of a corresponding semiconductor device, an appropriate device function adjusting means, in particular an appropriate fuse, may be provided on the semiconductor devices.

[0097] An appropriate laser fuse or e.g. an appropriate electrical fuse may, for instance, be used as a fuse.

[0098] When the fuse is shot, the corresponding device assumes e.g. a "master" function, and otherwise a "slave" function (or vice versa).

[0099] As is shown by means of the alternative embodiment for a semiconductor device system 1 illustrated in Figure 1b, the voltage supply means 3a of the first semiconductor device 2a may also be connected in any other way than in that illustrated in Figure 1a to the second semiconductor device 2b (or more exactly: the voltage supply means 3b of the second semiconductor device 2b (or the line or the connection, respectively, at which the voltage supply means 3b of the second semiconductor device 2b outputs the internal voltage generated thereby in the activated state).

[00100] For instance, in accordance with Figure 1b, the voltage supply means 3a of the first semiconductor device 2a may be connected - as described above - to a

semiconductor device pad 5a of the first semiconductor device 2a which - other than with the embodiment illustrated in Figure 1a - is connected to a corresponding contact of an interposer 9 (or to a corresponding leadframe connection 10 of the housing 4) by means of a bonding wire 6.

[00101] The interposer contact (or the leadframe connection 10) is connected to the pad 5b of the second semiconductor device 2b by means of a further bonding wire 6b, which is connected to the voltage supply means 3b of the second semiconductor device 2b (or the above-mentioned line or the connection, respectively, at which - in the activated state of the voltage supply means 3b of the second semiconductor device 2b - the internal voltage then generated thereby is output).

[00102] By this it can be achieved--similar as with the embodiment illustrated in Figure 1a - that in the second operating mode of the second semiconductor device 2b (e.g. during the standby mode and/or during the refresh mode) the voltage supply means 3a of the first semiconductor device 2a can - in addition to the voltage supply (internal voltage) for the first semiconductor device 2a - also provide the supply voltage (internal voltage) for the second semiconductor device 2b.

[00103] When - corresponding to the first embodiment - the voltage supply means 3b of the second semiconductor device 2b is correspondingly deactivated in the second operating mode, the operating current of the voltage supply means 3b can - corresponding to the embodiment illustrated in Figure 1a- be saved in the above-mentioned second operating mode (and thus, altogether, the currents required for operating the semiconductor devices 2a, 2b).

CLAIMS

What is claimed is:

1. (Currently Amended) A system ~~(1)~~ comprising:

a first semiconductor device ~~(2a)~~, and

a second semiconductor device ~~(2b)~~,

wherein the first semiconductor device ~~(2a)~~ and the second semiconductor device each comprise ~~comprises~~ a voltage supply device ~~means (3a)~~,

wherein ~~characterized in that~~ said voltage supply device ~~means (3a)~~ of said first semiconductor device ~~(2a)~~ is connected to said second semiconductor device ~~(2b)~~, so that said voltage supply device ~~means (3a)~~ of said first semiconductor device ~~(2a)~~ can provide a supply voltage for said second semiconductor device ~~(2b).~~ . and

wherein the system is adapted such that, in a first operating mode of the second semiconductor device, the voltage supply device of said second semiconductor device provides the supply voltage for the second semiconductor device, and, in a second operating mode of the second semiconductor device, the voltage supply device of said first semiconductor device provides the supply voltage for the second semiconductor device.

2. (Currently Amended) The system ~~(1)~~ according to claim 1, wherein said first semiconductor device ~~(2a)~~ and said second semiconductor device ~~(2b)~~ are arranged in ~~the~~ a same housing ~~(4)~~.

3. (Currently Amended) The system ~~(1)~~ according to claim 2, wherein said first and second semiconductor devices ~~(2a, 2b)~~ are arranged in said housing ~~(4)~~ in a stacked manner.

4. (Currently Amended) The system ~~(1)~~ according to claim 2, wherein said housing ~~(4)~~ is a plug mountable semiconductor device housing.

5. (Currently Amended) The system ~~(1)~~ according to claim 4, wherein said plug mountable semiconductor device housing is a Dual-In-Line (DIL) housing.

6. (Currently Amended) The system ~~(1)~~ according to claim 4, wherein said plug mountable semiconductor device housing is a Pin-Grid-Array (PGA) housing.

7. (Currently Amended) The system ~~(1)~~ according to claim 2, wherein said housing ~~(4)~~ is a surface mountable semiconductor device housing.

8. (Currently Amended) The system ~~(1)~~ according to claim 1, said system comprising one or several further semiconductor devices.

9. (Currently Amended) The system ~~(1)~~ according to claim 8, wherein said one or said several further semiconductor device(s) is/are arranged in ~~the same housing (4), in particular in the~~ a same semiconductor device housing as ~~, as are~~ said first and said second semiconductor devices ~~(2a, 2b)~~.

10. (Currently Amended) The system according to claim 8, wherein said voltage supply device ~~means (3a)~~ of said first semiconductor device ~~(2a)~~ is ~~additionally~~ also connected to said one or to said several further semiconductor device(s), so that said voltage supply device ~~means (3a)~~ of said first semiconductor device ~~(2a)~~ can additionally provide a supply voltage for said one or said several further semiconductor device(s).

11. (Currently Amended) The system ~~(1)~~ according to ~~any of~~ claim 8, wherein said first semiconductor device ~~(2a)~~ comprises a further voltage supply device ~~means~~ that is connected to said one or said several further semiconductor device(s), so that said further voltage supply device ~~means~~ of said first semiconductor device ~~(2a)~~ can provide a supply voltage for said one or said several further semiconductor device(s).

12. (Currently Amended) The system ~~(1)~~ according to claim 1, wherein said first and/or said second semiconductor devices ~~(2a, 2b)~~, and/or said one and/or said several further semiconductor devices are memory devices.

13. (Currently Amended) The system ~~(1)~~ according to claim 12, wherein said memory device is a table memory device or said memory devices ~~(2a, 2b)~~ are table memory devices, respectively.

14. (Currently Amended) The system ~~(1)~~ according to claim 13, wherein ~~said table memory device is a RAM table memory device or~~ said table memory device or said table memory devices are RAM table memory devices, respectively.

15. (Currently Amended) The system ~~(1)~~ according to claim 14, wherein said RAM table memory device is a DRAM table memory device or said RAM table memory devices are DRAM table memory devices, respectively.

16. (Currently Amended) The system ~~(1)~~ according to claim 13, wherein said table memory device is a ROM table memory device or said table memory devices are ROM table memory devices, respectively.

17. (Currently Amended) The system ~~(1)~~ according to claim 12, wherein said memory device is ~~a functional memory device~~ or said memory devices are ~~fundamental memory devices, respectively, in particular~~ programmable logic devices (PLDs) and/or programmable logic arrays (PLAs). ~~PLDs and/or PLAs.~~

18. (Currently Amended) The system ~~(1)~~ according to claim 1, wherein said voltage supply device ~~means (3a)~~ and/or said further voltage supply device ~~means~~ provide a voltage supply for said first semiconductor device ~~(2a)~~.

19. (Currently Amended) The system ~~(1)~~ according to claim 1, wherein said voltage supply means ~~(3a)~~ and/or said further voltage supply means generate(s) the respective supply voltage from an external voltage.

20. (Currently Amended) The system ~~(1)~~ according to claim 1, wherein said voltage supply device ~~means (3a)~~ and/or said further voltage supply device ~~means~~ are or comprise a voltage regulating device ~~means~~.

21. (Currently Amended) The system ~~(1)~~ according to claim 1, wherein said voltage supply device ~~means (3a)~~ and/or said further voltage supply device ~~means~~ are or comprise a charge pump.

22. (Canceled)

23. (Currently Amended) The system ~~(1)~~ according to claim 1 ~~22~~, wherein said voltage supply device ~~means (3b)~~ of said second semiconductor device ~~(2b)~~ is activated in the first operating mode, and wherein said supply voltage device ~~means (3b)~~ of said second semiconductor device ~~(2b)~~ is deactivated in the second operating mode.

24. (Currently Amended) The system ~~(1)~~ according to claim 1 ~~22~~, wherein the second operating mode is a standby mode.

25. (Currently Amended) The system ~~(1)~~ according to ~~claims~~ claim 1 ~~22~~, wherein the second operating mode is a refresh mode.

26. (Currently Amended) The system ~~(1)~~ according to claim 1 ~~22~~, wherein the first operating mode is a working mode, in particular a mode in which external access to the second semiconductor device ~~(2b)~~ is performed.

27. (Currently Amended) The system ~~(1)~~ according to claim 1, wherein ~~a device function adjusting means, in particular~~ an appropriate fuse[[,]] is provided on said first

and/or second semiconductor device(s) ~~(2a, 2b)~~, by means of which it is determined whether the corresponding semiconductor device ~~(2a, 2b)~~ is to assume the function of said first semiconductor device ~~(2a)~~ or the function of said second semiconductor device ~~(2b)~~.

28. (Currently Amended) The system ~~(1)~~ according to claim 1, wherein said voltage supply device ~~means (3b)~~ of said first semiconductor device ~~(2a)~~ is connected to a corresponding pad ~~(5a)~~ of said first semiconductor device ~~(2a)~~.

29. (Currently Amended) The system ~~(1)~~ according to claim 28, wherein said pad ~~(5a)~~ of said first semiconductor device ~~(2a)~~ is connected ~~to a corresponding pad (5b) of said second semiconductor device (2b), in particular~~ to a pad ~~(5b)~~ which said voltage supply device ~~means (3b)~~ of said second semiconductor device ~~(2b)~~ can be connected to.

30. (Currently Amended) The system ~~(1)~~ according to claim 29, wherein said pad ~~(5a)~~ of said first semiconductor device ~~(2a)~~ is connected directly to the corresponding pad ~~(5b)~~ of said second semiconductor device ~~(2b), in particular~~ by means of an appropriate bonding wire ~~(6)~~.

31. (Currently Amended) The system ~~(1)~~ according to claim 29, wherein said pad ~~(5a)~~ of said first semiconductor device ~~(2a)~~ is connected indirectly to the corresponding pad ~~(5b)~~ of said second semiconductor device ~~(2b), in particular~~ via an interposer ~~(9)~~.

32. (New) The system according to claim 12, wherein said memory devices are functional memory devices.

33. (New) The system according to claim 12, wherein said memory devices are fundamental memory devices.

ABSTRACT

The invention is directed to a system and method comprising a first semiconductor device and a second semiconductor device, wherein the first semiconductor device comprises a voltage supply means. characterized in that the voltage supply means of the first semiconductor device is connected to the second semiconductor device. so that the voltage supply means of the first semiconductor device can provide a supply voltage for the second semiconductor device

~~LIST OF REFERENCE SIGNS~~

~~1 semiconductor device system~~

~~2a semiconductor device~~

~~2b semiconductor device~~

~~3a voltage supply means~~

~~3b voltage supply means~~

~~4 semiconductor device housing~~

~~5a semiconductor device pad~~

~~5b semiconductor device pad~~

~~5c semiconductor device pad~~

~~5d semiconductor device pad~~

~~6 bonding wire~~

~~6a bonding wire~~

~~6b bonding wire~~

~~7a line~~

~~7b line~~

~~7c line~~

~~7d line~~

~~8 activating/deactivating control means~~

~~9 interposer~~

~~10 ——connection~~